

Government of Karnataka Department of Technical Education

C-25 Diploma in Electronics & Communication Engineering

Scheme of Studies

(Effect from the AY 2025-26)



Government of Karnataka

DEPARTMENT OF TECHNICAL EDUCATION

Curriculum Structure

I Semester Scheme of Studies

CI	Teaching Department	Course	Course Name	Hours per week		Total Contact	Credits	CIE Marks		Theory SEE Marks		Practice SEE Marks		Total	
51. No.		Code		L	Т	Р	Hours/week		Max	Min	Max	Min	Max	Min	Marks
					Integ	grated	Courses								
1	SC	25SC11I	Engineering Mathematics-I	4	0	4	8	6	50	20	50	20	-	-	100
2	CS	25CS01I	IT Skills	3	0	4	7	5	50	20	-	-	50	20	100
3	EE/EC	25EE01I	Fundamentals of Electrical & Electronics Engineering.	3	0	4	7	5	50	20	-	-	50	20	100
4	EC	25EC11I	Digital Electronics-I	4	0	4	8	6	50	20	50	20	-	-	100
					A	udit C	ourse								
5	EC	25EC12I	Environmental Sustainability	2	0	0	2	2	50	20	-	-	-	-	50
6 Personality Development NCC/NSS/YOGA/SPORTS			Studen Credits	Students are expected to engage in any one of these activities from 1 st semester to 6 th semester(No Credits)							No				
			Total	16	0	16	32	24	250	-	100	-	100	-	450
Note the o	: The course 25 course 25EE01I	EE01I shall be shall be	taught by faculty from the Ele red to faculty from the Electro	ctrical a nics & (& Elect Commi	ronics	(E&E) depart on (E&C) depa	ment. In tl artment. If	he even Sboth E	t that E &E and	&E facult E&C dep	y are not artments	available exist in th	in the ins ne institu	stitution, ition, the

course 25EE01I shall be taught by the E&C faculty.



Government of Karnataka DEPARTMENT OF TECHNICAL EDUCATION

Program	Electronics and Communication Engineering	Semester	1
Course Name	Digital Electronics-I	Type of Course	Integrated
Course Code	25EC11I	Contact Hours	8 hours/week (104 hours/semester)
Teaching Scheme	L: T:P :: 4:0:4	Credits	6
CIE Marks	50	SEE Marks	50 (Theory)

1. Rationale:

Digital electronics stems from its inherent advantages in reliability, versatility, scalability, and integration, reflecting its critical role in modern technology. Digital systems have transformed various industries, leading to advances in computing, communication and automation, making it a fundamental aspect of contemporary engineering and technology.

2. Course Outcomes: At the end of the Course, the student will be able to:

CO-01	Understand and perform arithmetic and conversion operations on different number systems.
CO-02	Formulate, simplify and implement simple logic functions using logic gates.
CO-03	Build and analyze various combinational circuits in a real time environment.
CO-04	Identify and utilize the suitable ICs for different applications.

3. Course Content

WEEK	CO	PO	Theory	Practice
			Introduction to Digital Electronics, Importance, and Its applications. https://youtu.be/DBTna2ydmC0?featur e=shared	1.Demonstrate number system and its conversion by using scientific calculator and verify theoretically.
1	1	1,2	 <u>Number Systems</u> Comparison between analog and digital signals with real-world examples. Number systems: Binary, Decimal and Hexadecimal. Relevance and examples. 	 2. Familiarize Digital IC Trainer Kit and do the following, Precautions to be taken while handling ICs. Analyze Pin diagram of an IC. Demonstrate the testing of an IC using an IC tester.

			https://youtu.be/FFDMzbrEXaE?fe	Demonstrate equivalent
			<u>ature=shared</u>	analog voltages for positive
				logic of logic 0 and logic 1
			<u>Conversion between number</u>	using Multimeter
			systems with examples	
			• Binary to decimal and vice	
			versa.	
			• Hexadecimal to decimal and	
			vice versa.	
			• Binary to nexadecimal and vice-versa	
-			(bitwise grouping only).	1 Deufeuru DCD e dditi eu suith
			Arithmetic operations and codes	1. Perform BCD addition with
			• Arithmetic operations.	simple examples.
			□ Addition and Subtraction on 4	2 Develop Binary to Gray code
			bit and 8 bit binary numbers	converter using IC 7486 and
			Addition and subtraction of	vice -versa.
			Heyadecimal numbers	
			nexadecimal numbers.	
2	1,4	1,2	• 1's & 2's complement of binary	
			numbers with examples.	
			• Representation of signed binary	
			numbers. Problems on subtraction	
			using 2's complement.	
			 Codes: BCD, Gray and ASCII- its 	
			features with examples,	
			applications	
			Digital Integrated Circuits	1. Verify the functionality of all
			https://study.com/academy/lesson/vid	the logic gates in the
			eo/digital-integrated-circuits-definition-	following ICs.
			types-examples.html	a. 7432 b. 7400
			 IC: Concept, Classification-Based on 	D. 7408
2	4	2.5	Scale of Integration.	2 Tabulate the parameters:
3			 IC- advantages and disadvantages 	Propagation delay fan-out
			 Logic-family concept, need and 	fan-in nower dissination
			types of logic families.	noise margin of the following
			Logic-family definitions:	ICs as per their Data Sheet.
			Propagation delay, fan-out, fan-in,	a. 7404
			speed and speed-nower product	b. 7486
			Boolean Algebra and Logic Cates:	1 Verification of Truth Table
			Boolean Algebra and Logic dates.	for all the logic gates
			Constants variables functions with	for an ene logie gates.
			examples	
			Boolean identities and Boolean	2. Verify De-Morgan's
			Laws.	Theorems using Logic
4	2,4	1,2	• Logic-gates (NOT, OR, AND,	gates.
			NOR, NAND, EX-OR and EX-NOR)	
			Symbol, function, expression and	
			truth-table.	
			• De-Morgan's Theorems with proof	
			and examples.	

			Universal Logic Gates & Boolean	1. Realization of NOT, OR,
5	2,4	1,2	 <u>expression simplification</u> Universal Logic Gates: Concept, examples. Realization of all logic gates using NAND Gate. Simplification of Boolean expressions using Boolean algebra. Build the logic circuit using logic gates for simplified Boolean expression 	AND gates using NOR Gates. 2. Realization of NAND, EX- OR, EX-NOR gates using NOR Gates.
6	2,4	1,2	 Boolean expression forms & <u>conversions</u> SOP and POS forms: Conversion into standard SOP forms. Conversion into standard POS forms. Translate SOP and POS expressions into truth-table. Convert truth-table to SOP and POS expressions. 	 Simplify a given SOP (3 variable) using Boolean laws and realize it using logic gates. Simplify a given POS (3 variable) using Boolean laws and realize it using logic gates.
7	2,4	1,2	 <u>Boolean expression simplification</u> <u>using K Map</u> Karnaugh Map: Need, Examples. Map grouping rules. Simplification of 2 and 3 variable Boolean expressions using K- map. Realize the above simplification using logic gates. 	 Reduce any 4 variable Boolean expressions using K-map. Realize and verify the above simplified Boolean expression using logic gates.
8	3,4	2,3,4	 <u>Combinational Circuits: Arithmetic</u> <u>Circuits</u> Features of combinational circuits, applications and examples. Half adder (HA): Concept, truth- table, logical expression, gate- level implementation. Full adder (FA): Concept, truth- table, logical expression, gate-level implementation. Half Subtractor (HS): Concept, truth-table, logical expression, gate-level implementation. Full Subtractor (FS): Concept, truth-table, logical expression, gate-level implementation. Full Subtractor (FS): Concept, truth-table, logical expression, gate-level implementation. 	 Construct and Verify Full Adder. Construct and Verify Full Subtractor.

9	3,4	2,3,4	 <u>Combinational Circuits: Adders &</u> <u>Comparators</u> Serial adders and Parallel adders: Concept, comparison & their applications. Working 8-bit serial adder. 3-bit parallel adder: Concept, Block diagram and its working. 1-bit magnitude comparator: Concept, Block diagram, truth- table logical expression gate- 	 Implement 3-bit parallel adder using IC 7483. Realize 1 bit comparator using logic gates.
10	3,4	2,3,4	 table, logical expression, gate- level implementation and application. <u>Combinational Circuits: Multiplexers</u> Multiplexers (Mux): Concept, general block diagram, No. of inputs to select line calculation. 2:1 Mux: Block diagram, truth-table, logical expression, gate-level implementation. 4:1 Mux: Block diagram, truth-table, 	 Implementation of 2:1 Mux using logic gates. Verify the functionality of 4:1 Mux using IC 74151.
11	3,4	2,3,4	 logical expression, gate-level implementation. Applications of Mux. <u>Combinational Circuits: De-Multiplexers</u> De-Multiplexers (De-Mux): Concept, general block diagram, No. of inputs to select line calculation. 1:2 De-Mux: Block diagram, truth- table, logical expression, gate-level implementation 1:4 De-Mux: Block diagram, truth- table, logical expression, gate-level implementation 	 Implementation of 1:2 De-Mux using logic gates Verify the functionality of 1:4 De-Mux using IC 74139.
12	3,4	2,3,4	 Applications of De-Mux. <u>Combinational Circuits: Encoders &</u> <u>Decoders</u> 4:2 Encoder: Block diagram, truth- table, logical expression, gate- level implementation, Applications. 2:4 Decoder: Block diagram, truth- table, logical expression, gate- level implementation, Applications. Decimal-to-BCD encoder: Logic diagram, working, truth-table and application. BCD-to-Decimal decoder: Logic diagram, working and truth-table. 	 Implement 4:2 Encoder using Logic gates. Implement 2:4 Decoder using Logic gates.

			<u>7 - Segment Display</u>	Implement BCD to 7 Segment decoder using a suitable IC.
13	3,4	2,4	 Seven-segment display: Principle and types. Identify and list ICs for 7-segment display and Decoder. BCD-to-seven segment decoder: Logic diagram, working and truth table (Only Anode Type) 	

NOTE

- 1. In practice sessions all video demonstrations should be followed by MCQ/Quiz/Subjective questions and evaluation has to be documented.
- 2. Online course completion certification to be done on relevant topics on Swayam/NPTEL/Infosys Springboard platforms or any other platform.
- 3. Problems statement to be collected from the relevant industries, resolve and submit it to the course coordinator.

4. References:

- i) Digital fundamentals Thomas L. Floyd, PEARSON EDUCATION publication, Eleventh edition – Global Edition, ISBN 10: 1-292-07598-8, ISBN 13:978-1-292-07598-3.
- ii) Digital Electronics principles and integrated circuits. Anil K. Maini. Wiley publications, first edition. ISBN:978-81-265-1466-3.
- iii) Digital principles and applications. Donald P Leach, Albert Paul Malvino, GoutamSaha, McGraw Hill Publisher, 7th edition, ISBN:978-0-07-014170-4.
 iv) Digital Systems-principles and applications. Ronald J. Tocci, Neal S.Widmer, Gregory L. Moss, Prentice Hall Publications, 8th edition, ISBN:0-13-085634-7.

v) Digital Computer Fundamentals, -Thomas C Bartee, McGraw-Hill Publisher, 4th edition. ISBN 0-07-003892-9.

Sl.No	CIE Assessment	Test Week	Duration (minutes)	Max marks	
1.	CIE-1Theory Test	4	90	50	
2.	CIE-2 Practice Test	7	180	50	Average of all
3	CIE-3 Theory Test	10	90	50	CIE=50 Marks
4.	CIE-4 Practice Test	13	180	50	
5	CIE-5 Portfolio evaluation of all the activities through Rubrics	1-13		50	
	·			Total	50 Marks

5. CIE Assessment Methodologies

Note: -

Portfolio evaluation includes average of (a) and (b)

- (a) Any one of the suggested activity model with report and presentation evaluated for 50 marks
- (b) Each laboratory exercise will be evaluated for a total of 50 marks. The evaluation will include the following components:
 - 1. Written description of the experiment in the observation book.
 - 2. Conducting the experiment and the associated learning outcomes.
 - 3. The results obtained from the experiment.

4. Corrections and evaluations of the experiment completed in the previous class, documented in the record book.

6. SEE - Theory Assessment Methodologies

SI. No	SEE – Theory Assessment	Duration	Exam Paper Max marks	Exam Paper Max Marks scale down to (Conversion)	Min marks to pass	
1.	Semester End Examination- Theory	3 Hours	100	50	20	

7. CIE Theory Test model question paper

Program		Electronics and Communication	Semester -1							
Course Na	ame	Digital Electronics-I		Test	I/III					
Course Co	ode		Duration	90 min	Marks	50				
Name of t	he Course Coo	ordinator:								
Note: Ans	wer any one fu	ll question from each section. Ea	ch full ques	tion carries e	equal marks.					
Q.No		Questions	estions Cognitive Level			Marks				
	Section - 1									
	a)Choose any from real er	7 3 Analog signals and any 2 Digit nvironment	L3	C01	05					
1	b) Convert the Hexadecima	e given Binary to Hexadecimal an al to Binary	d a given	L3	C01	5+5				
	c)Convert the to Binary	given Binary to Gray and the giv	ven Gray	L3	C01	5+5				
	a) Chart main signals?	advantages of digital signals over	r analog	L3	C01	05				
2	b) Convert the given Hexa	e given Decimal to Hexadecimal a Idecimal to Decimal.	and a	L3	C01	5+5				
	c) Perform ad subtraction	dition of the given 4-bit binary nu of the given 4 bit binary number	imber and r.	L3	CO1	5+5				
		Section - 2								

3	a) Mention and explain any 5 Boolean laws in Boolean	L2	CO2	5					
	b) Create a truth table for a 3-input AND gate and OR	L2	CO2	10					
	gate. c) Realize the basic logic function using only NAND or NOR gates.	L3	CO2	10					
	a) State and Interpret De-Morgan's theorem.	L2	CO2	5					
4	b) Express basic logic gates using only NAND gate?	L2	CO2	10					
Т	c) Simplify the given Boolean expression and implement using suitable Logic gates.	L3	CO2	10					
Note for the Course coordinator:									

1. Each question may have one, two or three subdivisions. Optional questions in each section carry the same weightage of marks, cognitive level and course outcomes. All questions must be framed under Understand (L2) & Apply (L3) cognitive level using Revised Bloom's Taxonomy.

Signature of the	Signature of the	Signature of the
Course Coordinator	HOD	IQAC Chairman

8. CIE Practice Test model question paper

Prog	ram	Electronics and communication EngineeringSeme					
Cours	ourse Name Digital Electronics-1 Tes						
Cours	se Code		Duration	180 min	Marks	50	
Name	e of the Cou	rse Coordinator:			<u> </u>	1	
	Questions CO						
Write-up for two experiments and conduction of any one experiment.						50	
Sche	me of assessr	nent					
a)	Writing the (Circuit diagram, tabular column, calculati	ons etc. fo	r two experii	nents.	20	
b)	Rig up and C	onduction of any one		-		15	
c) Result						05	
d)	Viva-voce					10	
				7	'otal Marks	50	

Signature of the Course Coordinator Signature of the HOD

Signature of the IQAC Chairman

9. Suggestive Activities for students:

The List is an Example and not inclusive of all possible activities of the course. Students and Faculty are encouraged to choose activities that are relevant to the topic. Note: Activity can be undertaken by either an individual or a team comprising up to 5 students.

	No Suggestive Activities for					
SI.NO.	students					
	Designing a Simple Digital lock.					
	To design and implement a digital lock using combinational logic that requires a specific					
	3-bit binary code to unlock.					
	Components:					
	* 7404 (NOT Gate IC)					
01	*7408 AND Gate IC					
	* 7432 (OP Cate IC)					
	* 7496 (VOP Cate IC)					
	* Proodboard jumper wires logic gwitches I EDs resistors					
	Breauboard, Jumper wires, logic switches, LEDS, resistors.					
	Designing a Simple Parity Checker.					
	To design a simple parity checker using combinational logic that determines whether a					
	binary number has even or odd parity.					
	Components:					
02	* 7404 (NOT Gate IC)					
	* 7408 (AND Gate IC)					
	* 7432 (OR Gate IC)					
	* Breadboard, jumper wires, logic switches, LEDs, resistors					
	Designing a Simple 4-bit BCD Adder.					
	To design and implement a 4-bit Binary-Coded Decimal (BCD) adder that adds two 4-bit					
	BCD numbers and produces a BCD result.					
	Components:					
03	* 7404 (NOT Gate IC)					
	* 7408 (AND Gate IC)					
	* 7432 (UR Gate IL)					
	* 7486 (XUK Gate IL)					
	Pagigning a Simula Binary to Desired Converter					
	Designing a Simple Binary-to-Decimal Converter.					
	To design and implement a binary-to-decimal converter using combinational logic that					
	converts a 4-bit binary number to its decimal equivalent, displaying the result on LEDS.					
	Components:					
	* 7404 (NOT Gate IC)					
04	* 7408 (AND Gate IC)					
	* 7432 (OR Gate IC)					
	* 7447 (BCD to 7-segment Decoder					
	IC) or equivalent					
	* 7-segment displays (if using a BCD decoder)					
	* Breadboard, jumper wires, logic switches, resistors.					
	Designing a Simple 4-bit Binary Alarm System.					
	To design and implement a basic 4-bit binary alarm system that triggers an alarm					
	when a specific 4-bit binary code is entered.					
	Components:					
05	7404 (NOT Gate IC)					
	7408 (AND Gate IC)					
	7432 (OR Gate IC)					
	7486 (XOR Gate IC)					
	Breadboard, jumper wires, logic switches, buzzer or LED (for alarm), resistors.					

10. Rubrics for Assessment of Activity (Qualitative Assessment)

Sl. No.	Dimension	Beginner	Intermediate	Good	Advanced	Expert	Students Score	
		10	20	30	40	50		
1		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	40	
2		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	30	
3		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	50	
4		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	20	
	Average Marks=(40+30+50+20)/4=35							

Note: Dimension and Descriptor shall be defined by the respective course coordinator as per the activities

11.Equipment/software list with Specification for a batch of 30 students

Sl.No.	Particulars	Specification	Quantity
01	Digital trainer kits.		15
02	IC tester, logic probes.		05
03	Digital Multimeters		15
04	Suitable ICs		20 Each
05	Patch cards (Different lengths)		300



Government of Karnataka DEPARTMENT OFTECHNICAL EDUCATION

Curriculum Structure

II Semester Scheme of Studies

	Teaching Department	Course Code	Course Name	Hours per week Total Contact		Total Contact Hours /week	CreditsCIE Marks			Theory SEE Marks		Practice SEE Marks		Total	
SI. No.		course coue		L	Т	Р	nours, week		Max	Min	Max	Min	Max	Min	Marks
	1				Integ	rated	Courses	1	1		1		1	I	
1	SC	25SC21I	Engineering Mathematics-II	4	0	4	8	6	50	20	50	20	-	-	100
2	ENG	25EG01I	Essential English Communication	4	0	4	8	6	50	20	-	-	50	20	100
3	ME	25ME02I	Computer Aided Engineering. Graphics	3	0	4	7	5	50	20	-	-	50	20	100
4	EC	25EC21I	Applied Electronics-1	4	0	4	8	6	50	20	50	20	-	-	100
	_		-		Αι	ıdit Co	ourse	_	_		_	_	-	-	
5	EC	25EC22T	Indian Constitution	2	0	0	2	2	50	20	-	-	-	-	50
6	Personality	Development	NCC/NSS/YOGA/SPORTS	Studer Credits	its are	expect	ed to engage i	n any or	ne of the	se acti	vities froi	m 1 st sem	ester to 6	th semest	ter (No
	1		Total	17	0	16	33	25	250	-	100	-	100	-	450



Government of Karnataka DEPARTMENT OF TECHNICAL EDUCATION

Program	Electronics & Communication	Semester	II
Course Name	Applied Electronics-I	Type of Course	Integrated
Course Code	25EC21I	Contact Hours	8 hours/week 104 hours/semester
Teaching Scheme	L:T:P :: 4:0:4	Credits	6
CIE Marks	50	SEE Marks	50 (Theory)

1. Rationale:

Applied electronics focuses on providing students with practical knowledge and hands-on skills that are directly applicable in the real-world electronic industry. It aims to equip students with the essential technical expertise needed to work as professionals in a variety of sectors that rely on electronic systems. Practical, focused and accessible topics for students to gain relevant skills that meet the needs of rapidly evolving industries.

By focusing on hands-on training, industry-relevant skills and emerging technologies, applied electronics programs ensure that students are ready to contribute to the workforce and tackle real-world challenges effectively. This education plays a crucial role in preparing the next generation of electronics professionals who will drive innovation and technological progress across a range of sectors.

2. Course Outcomes: At the end of the course, the student will be able to:

CO-01	Apply the knowledge of semiconductors to illustrate the functioning of basic electronic devices.
CO 02	Identify and select the electronic components, devices & instruments for any specific
CO-02	application.
	Demonstrate the switching and amplification application of the semiconductor
CO-03	devices.
CO 04	Design simple applications under real environments
CO-04	Design simple applications under rear environments.
CO-05	Test the designed circuit for an expected result/outcome, identify the problem and
	troubleshoot to obtain the desired result/outcome.

3. Course Content

WEEK	СО	РО	Theory	Practice
1	1,2	1,2,4,5	 Introduction to basic Electronics: Definition: Electronics. Atomic Structure, Structure of Elements, The Electron. Energy of an Electron 	 Video demonstration on atomic structure. Identification of Active and Passive components, Decade boxes (L, C and R).
			 S. Energy of an Electron, Valence Electrons, Free Electrons. 4. Find the valence electrons of at 	
			least 6 given elements	
			1. Bohr's Atomic Model, Energy Levels, Energy Bands.	1. Tabulate the electron configuration of Tetravalent (Silicon,
		1,2,4,5	2. Energy Bands in Solids.	Pentavalent.
2	1,2		3. Classification of Solids and Energy Bands.	2. Measurement of amplitude and frequency of sine,
			4. Atomic structure of Silicon & Germanium.	triangular, square waveform on CRO using signal generator.
			1. Applied Electronics - Introduction, simple	1. Practice Soldering Techniques.
			examples.	2. Diode as Center tapped Full
3		1,2,4,5	2. Bridge rectifier with Capacitive filter.	wave rectifier with Capacitive filter. Determine Vp, Vp-p, Time & Frequency of input
	1,2		3. Ripple factor and efficiency for the above rectifier - Simple problems.	signal using CRO. Measure Vrms and Vdc using multimeter and calculate
			4. Soldering - introduction, soldering techniques, types, steps for soldering.	output signal.

	1			
			1. Zener Diode - Construction, Symbol working principle	
			Symbol, working principle.	1.Construct & verify Zener diode as voltage regulator
			2. Applications - Zener diode	line regulation and load
			as a voltage regulator.	regulation.
4	1,2, 4	1,2,4,5	3. LED - Construction, Symbol,	2 Construct & verify forward
	4		working principle, applications.	& reverse bias characteristics
			4. Photo Diode - Construction,	of LED. Observe its light
			Symbol, working principle,	intensity for different
			applications.	voltages.
			1. BJT - Current operating	1. Demonstrate Numbering
5	2,4	1,3,4,5	device.	System of
			2. BJT Types- PNP and NPN,	Semiconductor Devices.
			Biasing of BJT.	Demonstrate different
			3. Types of configurations - CE,	packages of I ransistors.
			CC, CB.	of any NPN & PNP
			4 Need of DC lead line	transistors.
			operating point.	
			operating perm	
			1. Stabilization, thermal	
			runaway, heat sink	1. Test the Transistor and
			2. Voltage divider bias.	characteristics in CE
				configuration.
6	2,4	1,3,4,5	3. Definition of alpha, beta and	
			gamma and relationship	2. Test the Transistor and
			between them.	characteristics in CE
			4. Input and output	configuration.
			characteristics of CE.	5
			1. Applications of BJT -	
			List the applications of	
			real world	
				1 Turn ON and OFF a
			2. Transistor as a Switch –	BUZZER using a transistor.
			working.	
7	3,4	1,3,4,5	3. List the applications of	2. Transistor as a Switch for
			Transistors as amplification in	electromagnetic Relay.
			the real world.	
			4. Classification of Amplifiers	
			based on usage, frequency	
			capabilities, coupling methods	
			and mode of operation.	

8	3,4	1,3,4,5	 Single stage amplifier - Circuit diagram, working, various currents (I_b, I_c, I_e). Voltage gain of CE amplifier (No derivation). Frequency response of CE amplifier. Simple problems on gain. 	 Do It Yourself (DIY) a Single Stage Amplifier. Plot the frequency response of the CE amplifier.
9 3,4, 1,3,4,5		1,3,4,5, 7	 Concept of Multistage amplifier. Gain of the multistage amplifier. Direct on whether which and 	 Build and test the performance of the Direct coupled two stage amplifier and Plot the frequency response. DIY - Make an earphone
			 3. Direct coupled amplifier - Circuit diagram, operation 4. Direct coupled amplifier - frequency response. 	for Mobile.
10	2,4, 5	1,3,4,5, 7	 RC coupled amplifier – Circuit diagram, operation and frequency response. Advantages, Disadvantages of RC coupled amplifier. Applications of RC coupled amplifiers. Comparison of Different Types of Coupling. 	1. Build and test the performance of the RC coupled two stage amplifier and Plot the frequency response.
11	2,4, 5	1,3,4,5, 7	 Voltage operating device - FET – Introduction of FET, Types of FET. JFET - Symbol, Salient features of JFET. Principle and working of JFET (N channel) Importance of JFET, Difference between JFET and BJT. 	 Drain Characteristics of N- channel JFET. Transfer Characteristics of N- channel JFET.

12	2,4, 5	1,3,4,5, 7	 JFET parameters: Drain resistance (rd), Transconductance (gfs), Amplification Factor(μ) and relation among JFET parameters (No Derivation), JFET applications MOSFET - Types, Symbol. Construction, working principle and characteristics of Depletion MOSFET. 	 Precautions to be followed for handling MOSFETs. Demonstrate MOSFET as a switch to control an LED. Demonstrate MOSFET as a switch to control a DC motor.
			4. Construction, working	
			principle and characteristics of	
			Enhancement MOSFET.	

			1. D-MOSFETs versus JFETs	
			2. D-MOSFETs versus E- MOSFETs	1. Construct AND/OR gate using any transistors.
13	2,4, 5	1,3,4,5, 7	3. Introduction to CMOS, features, working and applications.	2. Construct NAND/NOR gate using any transistors.
			4. CMOS inverter: Schematic diagram, working and application.	

Note:

- 1. In practice sessions all video demonstrations should be followed by MCQ/Quiz/ Subjective questions and evaluation has to be documented.
- 2. Online course completion certification to be done on relevant topics on Swayam/NPTEL/Infosys Springboard platforms or any other platform.
- 3. Problem statement to be collected from the relevant industries, resolve and submit it to the course coordinator.

4. References:

- 1. Principles of Electronics, Rohit Mehta & V K Mehta, S. Chand Publishing ISBN: 9788121924504
- 2. Fundamentals of Electrical and Electronics Engineering, B. L. Theraja, S. Chand and Company. REPRINT 2013, ISBN 8121926602
- 3. "A Textbook of Applied Electronics" by R. S. SEDHA.

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- 5. Electronic Devices and Circuits, David A. Bell, Oxford University Press, ISBN: 9780195693409.
- 6. <u>https://youtube.com/shorts/YpXy5gGRncY?feature=shared</u>
- 7. <u>https://youtu.be/enwdrtef7r0?feature=shared</u>
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- 10. <u>https://youtu.be/lFdtH9CHlfA?feature=shared</u>
- 11. https://youtube.com/shorts/hUW_o0u5X6c?feature=shared
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5. CIE Assessment Methodologies

Sl.No	CIE Assessment	Test Week	Duration (minutes)	Max marks		
1.	CIE-1 Theory Test	4	90	50		
2.	CIE-2 Practice Test	7	180	50	Average	
3	CIE-3 Theory Test	10	90	50	of all CIF=50	
4.	CIE-4 Practice Test	13	180	50	Marks	
5	CIE-5 Portfolio evaluation of all the activities through Rubrics	1-13		50		
		·		Total	50 Marks	

Note:- Portfolio evaluation includes average of (a) and (b)

(a) Any one of the Suggested activity model with report and presentation evaluated for 50 marks

- (c) Each laboratory exercise will be evaluated for a total of 50 marks. The evaluation will include the following components:
 - 1. Written description of the experiment in the observation book.
 - 2. Conducting the experiment and the associated learning outcomes.
 - 3. The results obtained from the experiment.

4. Corrections and evaluations of the experiment completed in the previous class, documented in the record book.

6. SEE - Theory Assessment Methodologies

SI. No	SEE – Theory Assessment	Duration	Exam Paper Max marks	Exam Paper Max Marks scale down to (Conversion)	Min marks to pass
1.	Semester End Examination- Theory	3 Hours	100	50	20

7. CIE Theory Test model question paper

Program		Electronics & Com	Electronics & Communication Engg			
Course Name		Applied Electronic	s - I		Test	I/III
Course Co	ode	25EC21I	Duration	90 min	Marks	50
Name of t	the Course Co	ordinator:				
Note: Ans	wer any one fu	Ill question from each	section. Each full qu	estion carrie	es equal mark	KS.
Q.No	Questions			Cognitive Level	Course Outcome	Marks
		Se	ction - 1			
	a) Realize a amplifiers.	multistage amplifier u	sing individual	L3		5 M
1	b) Identify a device whic	nd explain a two term h works as voltage reg	inal electronic gulator.	L3	CO 1	10 M
	c) Demonstr applications	strate transistors as an amplifier and list its L2				10 M
	a) Interpret b) Explain t	: JFET as a voltage con he concept of field effe	L2	CO 1	5 M	
2	analyze ł	now it controls current	L3		10 M	
	of N Chan	Channel JFET.				10 M
		Se	ction - 2		I	
	a) Base widt collector is t	ch of the transistor is t hick. Infer your answe	hin and the er.	L2		5 M
3	b) Discuss the	ne importance of heat	sinks in	L3	CO 2	10 M
	c) Illustrate	the working of NPN/F	NP transistor	L2		10 M
	a) Develop a	in Inverter using CMO	S.	L3		5 M
	b) Explain w and list it	L2	CO 2	10 M		
4	c) Illustrate	the transistor as a swi	itch.	L2		10 M
Note for t	the Course coo	ordinator:			. 1	

1. Each question may have one, two or three subdivisions. Optional questions in each section carry the same weightage of marks, cognitive level and course outcomes.

2. All questions must be framed under Understand (L2) & Apply (L3) cognitive level using Revised Bloom's Taxonomy.

Signature of the Course Coordinator Signature of the HOD

Signature of the IQAC Chairman

8. CIE Practice Test model question paper

Program Electronics & Communication					II
Course Name	Applied Electronics - I			Test	II/IV
Course Code	25EC21IDuration180 min				50
Name of the Cou	irse Coordinator:			·	·
	Questions			CO	Marks
Write up for two experiments and conduction of any one experiment. CO 4,CO 5					50
Scheme of asse a) Writing the b) Rig up and c) Troublesh d) Result/Ou e) Viva-voce	<u>essment</u> Circuit diagram, tabular column, calcu Conduction of any one ooting tput	llations etc. f	or two experi	iments.	20 M 10 M 05 M 05 M 10 M
			To	tal Marks	50

Signature of the	Signature of the	Signature of the
Course Coordinator	HOD	IQAC Chairman

9. Suggestive Activities:

The List is an example and not inclusive of all possible activities of the course. Students and Faculty are encouraged to choose activities that are relevant to the topic.

Note: Activity can be undertaken by either an individual or a team comprising up to 5 students.

SI.N o.	Suggestive Activities
01	Smoke detector application
02	Fire Alarm/detector application.
03	Clapp/sound detector application
04	Intruder detector
05	LED serial-sets
06	Simple 10 Watt Audio Amplifier
07	And all such simple circuits/projects that have scope to integrate multiple concepts learnt and for which circuits/boards/components are easily available.

Sl.	Dimension	Beginner	Intermediate	Good	Advanced	Expert	Students Score
No.		10	20	30	40	50	
1		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	40
2		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	30
3		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	50
4		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	20
	Average Marks=(40+30+50+20)/4=35						35

10. Rubrics for Assessment of Activity (Qualitative Assessment)

Note: Dimension and Descriptor shall be defined by the respective course coordinator as per the activities

11. Equipment/software list with Specification for a batch of 30 students

Sl. No.	Particulars	Specification	Quantity
1	Regulated Power Supply (Single) with short-	1A/2A 0-30V	15
1	circuit protection		
2	Regulated Power Supply (Dual) with short-	1A/2A 0-30V	15
2	circuit protection		
3	Function Generator	0-10MHz	15
4	Dual Trace Oscilloscope	20MHz	15
5	Digital multimeters.		20
6	Decade resistance boxes		15
7	Decade capacitance boxes		15
8	Decade inductance boxes		15
9	LCR meter		05
	Electronic components/Consumables		
	resistors, inductors, capacitors, transformers,		
10	hook up wires, SCR, MOSFET, DIAC, TRIAC,		20 each
	BJT, JFET, diode, Zener diode, soldering lead		
	Etc.		
	Bread boards, Soldering Gun, Tag Board,		
11	General purpose PCB, 9V battery cells,		20 each
	Bulbs.		